Study of Low-Power Circuits for Thermoelectric Harvesting in 28 nm FDSOI CMOS Technology

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***Abstract*—Energy harverters such as thermoelectric generators (TEGs) or photovoltaic cells provide solutions for battery-free sensor network or healthcare systems. This paper studies low-power circuits for energy harvesting applications, in particular the behavior and design of both start-up and charge pump circuits. Simulation results using a 28 nm fully-depleted silicon-on-insulator (FD-SOI) CMOS technology show that the designed harvesting system can operate at minimum input voltage of 200 mV and frequency of 2 kHz.**

***Index Terms*—Energy harvesting, charge pump, ring oscillator, start-up circuit, thermometric generator.**

I. Introduction

In view of the continuous growing of Internet-of-Things (IoT) applications, ultra low power (ULP) has received increasing attention in system-on-chip (SoC) since several circuits require prolonged battery life [1], [2]. The ever increasing demand for energy makes energy harvesters an efficient solution for ULP SoCs. Among others harvesters, the thermoelectric generator (TEG) presents unique capabilities, such as its reported durability of 30 years, it can be manufactured to be as small as 0.5 mm × 0.5 mm × 100 μm and has a low deploying cost compared to large generators or batteries [3].

This paper presents a study of low-power circuits for thermoelectric harvesting applications. The analysis, design and simulation of the start-up and charge pump circuits are carried out using a 28 nm FD-SOI CMOS Process. The paper is organized as follows. Section II shows the proposed energy harvesting system to operate down to 200 mV, which aims to be powered by a TEG. Section III advances analytical expressions, based on charge balance, to estimate the charge pump output voltage with and without load. Section IV presents simulation results. Concluding remarks are made in Section V.

II. Proposed System

This work aims at the study of a low-power system for energy harvesting applications. As shown in Fig. 1, the proposed model is divided into five circuits: thermometric generator (TEG), ring oscillator (OSC), complementary clock generator (CCG), charge pump doubler (CP) and linear regulation (LR). However, this paper focuses on the study of two operational blocks of this scheme: the charge pump doubler block and the start-up block composed by ring oscillator and complementary clock generation circuits.

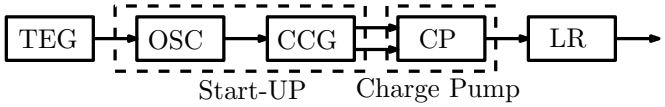

Fig. 1. Energy harvesting system.

A. Start-UP Block

The Start-UP Block is composed by two circuits: ring oscillator and complementary clock generator. With the purpose of producing the clock signal, the ring oscillator was implemented with fifteen cascaded dynamic leakage-suppression (DLS) [4] inverters. It is worth mentioning that in order to produce a clock signal an odd number of inverters are required in cascades, as seen in [5]. The output of the ring oscillator is connected to the CCG block in order to generate the complementary clock waves, which are required by the charge pump circuit.

As mentioned, the CCG block has the function of producing two complementary clock waves. With this purpose, a circuit composed for two DLS nand gates and DLS inverters was implemented. Similar to a Flip-Flop type D circuit, the clock signal generated by the OSC block is connected to one of the both DLS inputs nand gates. However before being connected to one of them it passes trough an DLS inverters. After passing through an even number of cascaded DLS inverters the output of each DLS nand gate is connected to the input of the other. Note that unlike the ring oscillator circuit the number of inverters connected in cascades in this case is even and not odd, as the interest here is to delay the output signals of the DLS nands gates. These outputs are called CLK and $\overline{\text{CLK}}$ and are used to initialize the Charge Pump Block. The Start-UP Block is shown in Fig. 2.

B. Charge Pump Block

The charge pump is implemented by the classical Charge Pumper Doubler which is depicted in Fig. 3. Transistors X_{N1}, X_{N2}, X_{P1} and X_{P2} behave as cross-connected switches and are driven by clock phase waves, CLK and $\overline{\text{CLK}}$, generated by start-up block [6]. The capacitors C_{f1} and C_{f2} are called fly capacitors and are responsible for the transfer of charge from the input to the output. However the capacitor C_{OUT}, denominated output capacitor, does not has influence in this

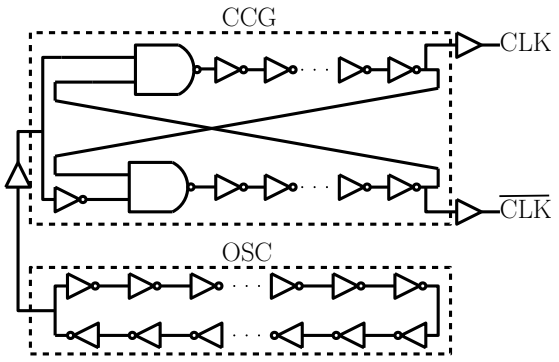

Fig. 2. Schematic of the start-up circuit.

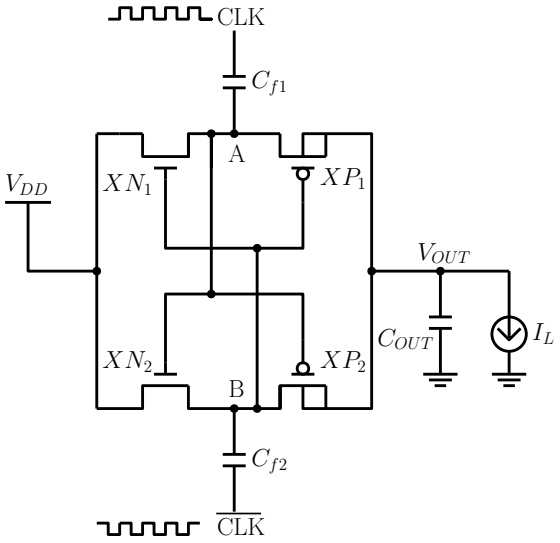

Fig. 3. Schematic of the charge pump circuit [6].

transfer of the charge, it has influences in the initialization of the circuit [7].

For understanding the operation of the doubler it is necessary the analysis of the circuit behavior during the clock phases. The analysis can be described in two cases, first when there is no load at the output of the charge pump and second when there is a load connected at the output. In order to analyze the charge pump doubler, we divided its behavior in two phases as described below.

1) Phase 1: In the first phase it is considered that the pulse CLK is LOW, resulting in the activation and deactivation of the transistors X_{P2} and X_{N2}, respectively. As CLK is LOW, the pulse $\overline{\text{CLK}}$ is HIGH, resulting in the activation and deactivation of the transistors X_{P1} and X_{N1}, respectively. Consequently, the capacitor C_{f1} is loaded in V_{DD} by node A and the capacitor C_{f2} is discharged in the node V_{OUT}. Therefore, the capacitor C_{OUT} is loaded in V_{DD}.

2) Phase 2: In the second phase of analysis it is considered that the pulse CLK is HIGH, resulting in the activation and deactivation of the transistors X_{N2} and X_{P2}, respectively. As CLK is HIGH, the pulse $\overline{\text{CLK}}$ is LOW, resulting in the activation and deactivation of the transistors X_{N1} and X_{P1}, respectively. Consequently, the capacitor C_{f2} is loaded in V_{DD} by node B and the capacitor C_{f1} is discharged in the node V_{OUT}. Therefore, the capacitor C_{OUT} is loaded in $2V_{DD}$ [6]. In the next section, charge balance analyses were derived in order to obtain on analytical mode of the output voltage as a function of circuits parameters.

III. Charge Balance Analysis

Assuming that, in transient mode, the charge of the doubler is conserved from the one phase to other during of the switching period, it can be derived the charge balance analysis of the circuit. This analysis is based on the principle of the charge conservation law [7],

$$Q_{IN} = Q_{OUT} \tag{1}$$

where, Q_{IN} corresponds to the initial charge at Phase 1 and Q_{OUT} the final charge at Phase 2.

A. Charge Pump Doubler With Output Load

The charge balance analysis of the charge pump doubler with output load will be divided in two phases described below.

1) Phase 1: In the first phase, the doubler circuit with output load behaves analogously to the circuit without a load at its output. Therefore, the transistors X_{P2} and X_{N1} will be activated and the transistors X_{P1} and X_{N2} will be deactivated, as in the previous case. Making the charge balance analysis of the capacitors C_{f1} and C_{OUT}, we obtain

$$Q_{IN} = Q_{C_{f1}} + Q_{OUT}. \tag{2}$$

It is known that the charge on a capacitor is given by

$$Q = CV. \tag{3}$$

Replacing (3) in (2), we obtain

$$Q_{IN} = (V_{DD} - 0)C_{f1} + V_{OUT_1}C_{OUT}. \tag{4}$$

2) Phase 2: In order to include the load effects, in a simple way, we can consider that it instantaneously consumes a portion of the charge. With respect to the transistors, they behave as in the case with no load at the output, that is, the transistors X_{P2} and X_{N1} will be deactivated and the transistors X_{P1} and X_{N2} will be activated. When analyzing the charge on the capacitors C_{f1}, C_{OUT} and on the current source, we have

$$Q_{OUT} = (V_{OUT_2} - V_{DD})C_{f1} + V_{OUT_2}C_{OUT} + Q_{I_L}. \tag{5}$$

By differentiating (3) we can model the load at the output as a current source as $I_L = C\Delta V/\Delta t$. Since Δt^{-1} represents the operation frequency (f) and considering that each fly capacitor operates at all half period, yields

$$C\Delta V = \frac{I_L}{2f}. \tag{6}$$

Therefore, by substituting (6) into (5),we obtain

$$Q_{OUT} = (V_{OUT_2} - V_{DD})C_{f1} + V_{OUT_2}C_{OUT} + \frac{I_L}{2f}. \tag{7}$$

By applying the charge conservation law, in Eq. (1), in Phase 1 - Phase 2 transition, we find

$$V_{DD}C_{f1} + V_{OUT_1}C_{OUT} = (V_{OUT_2} - V_{DD})C_{f1} + V_{OUT_2}C_{OUT} + \frac{I_L}{2f}. \quad (8)$$

After a long time (approximately 64 ms), the output voltages of the two phases are the same, and the final state of the output result in

$$V_{OUT} = 2V_{DD} - \frac{I_L}{2fC_{f1}}. \quad (9)$$

B. Charge Pump Doubler Without Output Load

To the charge balance analysis of the charge pump doubler without output load will be used the parsing described in previous Section. Making the charge balance analysis of the capacitors C_{f1} and C_{OUT} in the first phase operation of the circuit, we have again the Eq. (4). Applying the same analysis for the second phase, we obtain

$$Q_{OUT} = (V_{OUT_2} - V_{DD})C_{f1} + V_{OUT_2}C_{OUT}. \quad (10)$$

By applying the charge conservation law, in Eq. (1), in Phase 1 - Phase 2 transition, we find

$$V_{DD}C_{f1} + V_{OUT_1}C_{OUT} = (V_{OUT_2} - V_{DD})C_{f1} + V_{OUT_2}C_{OUT}. \quad (11)$$

After a long time, the output voltages of the two phases are the same, and the final state of the output result in

$$V_{OUT} = 2V_{DD}. \quad (12)$$

Note that the result obtained in the charge balance analysis of the circuit without load on the output is similar to the result obtained in Subsection II-B.

IV. Simulation and Results

The results obtained by simulating the two blocks under analysis of the proposed system are presented in the following subsections.

A. Start-UP Block Results

As mentioned in Subsection II-A the start-up block consists of two circuits, the ring oscillator and the complementary clock generator. In this subsection we analyze the behavior of the block at four voltage levels. The oscillation frequency of the clock signal generated by the proposed start-up block is shown in the Table I. Note that, the oscillation frequency decays with increasing voltage.

Fig.4 shows the clock signal produced by the ring oscillator with V_{DD} of 200 mV. Fig. 5 displays the simulations results of the complementary clock signals, CLK and $\overline{\text{CLK}}$, which are necessary to the proper charge pump operation. This signals are generated by the CCG circuit showed in Fig. 2.

TABLE I
Simulated frequencies with respect to different input voltages

V_{DD} (mV)	Frequency (kHz)
200	2.00
300	1.57
400	1.25
500	1.00

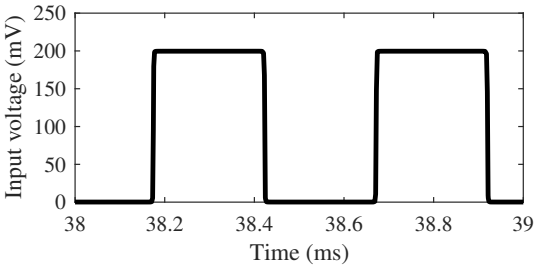

Fig. 4. Clock signal using V_{DD} = 200 mV.

B. Charge Pump Block Results

This section presents comparisons between the simulated results and analytical ones derived in Section III. The simulated resistance of the transistors with respect to their widths, are presents in Table II. The NMOS and PMOS transistors for the design of the charge pump circuit were determined. For this we used the sizes that have approximately the same resistances. In this case, we chose NMOS with 100 nm and PMOS with 400 nm of width. The comparison of the output voltages obtained by simulations and using Eq. (12) for different voltage levels are shown in Table III. Note that the output voltage does not double as expected, after being close to twice the input voltage. This indicates that the circuit is losing charge throughout the switching. The graphic illustrated in Fig. 6 shows simulated output voltages over time.

TABLE II
Resistance related to different transistor widths using L = 32 nm

W (nm)	R_{ON} of NMOS (MΩ)	R_{ON} of PMOS (MΩ)
100	2.37	25.12
200	1.42	6.1
300	1	2.98
400	0.78	1.9
500	0.64	1.37
600	0.54	1.06
700	0.47	0.87
800	0.41	0.73
900	0.36	0.63
1000	0.33	0.61
2000	0.17	0.27
3000	0.11	0.17

The results of the simulated output voltages and the other ones produced by Eq. (9), using different input voltages, are shown in Table IV. Fig. 7 shows the simulation results using load of 1 nA at the output. The difference between simulated

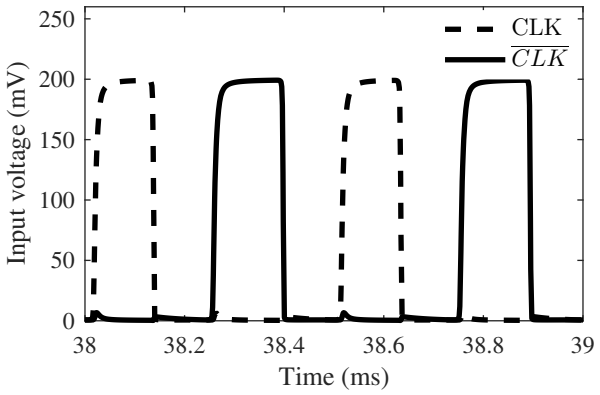

Fig. 5. Complementary clock signals using V_{DD} = 200 mV.

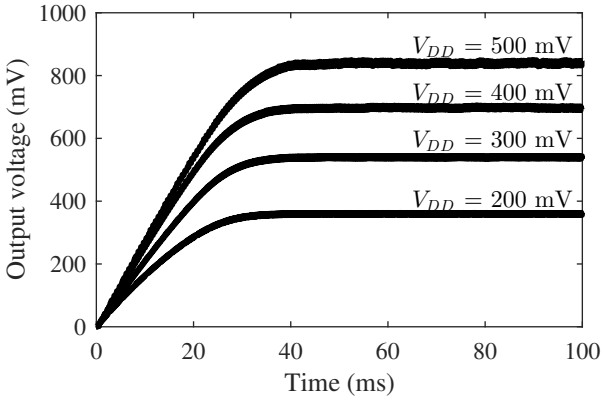

Fig. 6. Transient response of the output voltage.

TABLE III
COMPARISON BETWEEN THE V_{OUT} OBTAINED BY THE EQ. (12) AND THE SIMULATION

V_{DD} (mV)	V_{OUT} by Eq. (12) (mV)	Simulated V_{OUT} (mV)
200	400	362.17
300	600	534.61
400	800	689.84
500	1000	847.32

and analytical results are shown in Table IV. The difference between simulated and analytical results is explained by the charge losses in the simulated circuit, which are not considered in the modeling. As can be observed, a charge pump gain of 1.61 is obtained when input voltages of 500 mV is used.

TABLE IV
COMPARISONS BETWEEN V_{OUT} OBTAINED BY EQ. (9) AND SIMULATIONS

V_{DD} (mV)	V_{OUT} by Eq. (9) (mV)	Simulated V_{OUT} (mV)
200	350	278.2
300	536.31	511.64
400	720	672
500	900	805.04

V. CONCLUSION

In this paper, the start-up and charge pump circuits for thermoelectric harvesting were carried-out by using a 28 nm FD-SOI CMOS technology. Simulation results shown that the proposed system is able to operate at minimum input voltage of 200 mV and at a switching frequency of 2 kHz (ring oscillator). The study of using additional charge pump stages to increase the output voltage, and a linear regulator in order to produce the complete energy harvesting system showed in Fig. 1, are the future directions of this research.

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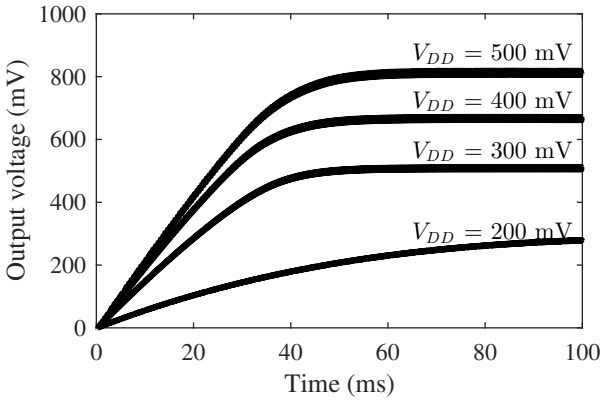

Fig. 7. Transient response of the output voltage using a load of 1 nA.

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